What is claimed is:

1. An information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said information processor comprising:

a voltage controlling module for causing said instruction execution module to execute a voltage reduction instruction for placing said central processing unit into a low-voltage operation mode in which the operating voltage of said central processing unit is lowered from the operating voltage in said normal mode when said central processing unit switches from said normal mode to said execution halt mode; and

a mode controlling module for placing said central processing unit into a low-voltage halt mode in which said instruction execution module is halted under the operating voltage for said low-voltage operation mode when said voltage controlling module places said central processing unit into said low-voltage operation mode.

2. The information processor according to Claim 1, wherein: after said voltage controlling module causes said instruction execution module to execute said voltage reduction instruction, said voltage controlling module causes said instruction execution module to execute a halt grant instruction for sending a halt grant signal to said mode controlling module, said halt grant signal allowing said instruction execution module to halt; and said mode controlling module places said central processing unit into said low-voltage halt mode when said mode controlling module receives said halt grant signal.

3. The information processing module according to Claim 1, wherein: when said central processing unit receives an interrupt request for resuming said instruction execution module in said low-voltage halt mode, said mode controlling module places said central processing unit into said low-voltage operation mode; and when

said mode controlling module places said central processing unit into said low-voltage operation mode in response to said interrupt request, said voltage controlling module causes said instruction execution module to execute a voltage raise instruction for changing the operating voltage of said central processing unit to the operating voltage in said normal mode and places said central processing unit into said normal mode.

4. The information processor according to Claim 3, wherein said interrupt request is an interval timer interrupt provided periodically to said central processing unit to cause said instruction execution module to execute periodically a set of instructions for detecting an executable process; and when said mode controlling module places said central processing unit into said low-voltage operation mode in response to said interval timer interrupt, said voltage controlling module causes said instruction execution module to execute said voltage raise instruction to place said central processing unit into said normal mode, provided that an executable process is detected; and if no executable process is detected, said mode controlling module places said central processing unit into said low-voltage halt mode.

5. The information processor according to Claim 4, wherein after said instruction execution module completes the process detected in response to said interval timer interrupt, said voltage controlling module causes said instruction execution module to execute said voltage reduction instruction if the time between the completion of said detected process and reception of the next interval timer interrupt exceeds a predetermined value or retains the operating voltage of said central processing unit without causing said instruction execution module to execute said voltage reduction instruction if the time between the completion of said detected process and reception of the next interval timer interrupt does not exceeds the predetermined value.

6. The information processor according to Claim 1, wherein said central

processing unit further has a voltage reduction mode in which said instruction execution module is halt at a low operating voltage compared with the operating voltages in said low-voltage operation mode and said low-voltage halt mode; and when said central processing unit is shifted from said normal mode to said voltage reduction mode, said voltage controlling module retains the operating voltage in said normal mode without causing said instruction execution module to execute said voltage reduction instruction; and said mode controlling module causes said central processing unit to shift from said normal mode to said voltage reduction mode.

7. The information processor according to Claim 1, wherein when said voltage controlling module causes said central processing unit to shift from said normal mode to said low-voltage operation mode, said voltage controlling module operates said central processing unit and places said central processing unit into an intermediate-voltage operation mode in which the operating voltage is lower than the operating voltage in said normal mode and higher than the operating voltage in said low-voltage operation mode and then places said central processing unit into said low-voltage operation mode.

8. An information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said information processor comprising:

a frequency controlling module for causing said instruction execution module to execute a frequency reduction instruction for placing said central processing unit into a low-frequency operation mode in which the operating frequency of said central processing unit is lowered from the operating frequency in said normal mode when said central processing unit switches from said normal mode to said execution halt mode; and

a mode controlling module for placing said central processing unit into a low-frequency halt mode in which said instruction execution module is halted under

the operating frequency for said low-frequency operation mode when said frequency controlling module places said central processing unit into said low-frequency operation mode.

9. A program for controlling an information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said program causing said information processor to function as:

a voltage controlling module for causing said instruction execution module to execute a voltage reduction instruction for placing said central processing unit into a low-voltage operation mode in which the operating voltage of said central processing unit is lowered from the operating voltage in said normal mode when said central processing unit switches from said normal mode to said execution halt mode; and

a mode controlling module for placing said central processing unit into a low-voltage halt mode in which said instruction execution module is halted under the operating voltage for said low-voltage operation mode when said voltage controlling module places said central processing unit into said low-voltage operation mode.

10. A program for controlling an information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said program causing said information processor to function as:

a frequency controlling module for causing said instruction execution module to execute a frequency reduction instruction for placing said central processing unit into a low-frequency operation mode in which the operating frequency of said central processing unit is lowered from the operating frequency in said normal mode

when said central processing unit switches from said normal mode to said execution halt mode; and

a mode controlling module for placing said central processing unit into a low-frequency halt mode in which said instruction execution module is halted under the operating frequency for said low-frequency operation mode when said frequency controlling module places said central processing unit into said low-frequency operation mode.

11. A storage medium on which the program according to one of Claim 9 or 10 is stored.

12. A control method for controlling an information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said method comprising:

causing said instruction execution module to execute a voltage reduction instruction for placing said central processing unit into a low-voltage operation mode in which the operating voltage of said central processing unit is lowered from the operating voltage in said normal mode when said central processing unit switches from said normal mode to said execution halt mode; and

placing said central processing unit into a low-voltage halt mode in which said instruction execution module is halted under the operating voltage for said low-voltage operation mode when said central processing unit is placed into said low-voltage operation mode.

13. A control method for controlling an information processor including a central processing unit having an instruction execution module, said central processing unit having a normal mode for operating said instruction execution module and an execution halt mode for halting said instruction execution module; said method

comprising:

causing said instruction execution module to execute a frequency reduction instruction for placing said central processing unit into a low-frequency operation mode in which the operating frequency of said central processing unit is lowered from the operating frequency in said normal mode when said central processing unit switches from said normal mode to said execution halt mode; and

placing said central processing unit into a low-frequency halt mode in which said instruction execution module is halted under the operating frequency for said low-frequency operation mode when said central processing unit is placed into said low-frequency operation mode.